PROCESSOR INSTRUCTION SET SIMULATION
POWER ESTIMATION METHOD

ABSTRACT OF THE DISCLOSURE

A plurality of compound Single Instruction/Multiple Data instructions in the form of vector arithmetic unit instructions and vector network unit instructions are disclosed. Each compound Single Instruction/Multiple Data instruction is formed by a selection of two or more Single Instruction/Multiple Data operations of a reduced instruction set computing type, and a combination of the selected Single Instruction/Multiple Data operations to execute in a single instruction cycle to thereby yield the compound Single Instruction/Multiple Data instruction.